REMARKS

The Office Action dated October 21, 2005, in this Application has been carefully considered. Claims 1-10, 12-14, 16, 18-19, and 21-23 are pending. The above amendments and the following remarks are presented in a sincere attempt to place this Application in condition for allowance. Claims 1-10, 12-14, 16, 18-19, and 21 have been amended, and claims 22-23 added, in this Response. Claims 11, 15, 17, and 20 have been cancelled in this Response. Reconsideration and allowance are respectfully requested in light of the above amendments and following remarks.

The Specification has been amended to correct a few errors in the present Application. The list of cross-referenced patent applications has also been amended to accurately represent the list of related patent applications. Applicant submit that these amendments to the specification do not provide new subject matter, and that these amendments are supported by the original Application as filed.

Claim 13 was objected to due to recitation of "the second cache" that lacked antecedent basis. Applicant has amended claim 13 herein, and believes claim 13 as amended herein is in condition for allowance.

Claim 1 was provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of co-pending application 10/655367, and in view of Arimilli et al. (US Patent No. 6,425,058).

In response thereto, Applicant notes that claim 1 is amended herein to recite:

1. A computing system, comprising:
   a plurality of memory regions each having a different address range and a corresponding class identifier;
   a range register coupled to receive an address and configured to produce: (i) the class identifier corresponding to the memory region having an address range that includes the received address, or (ii) a default class identifier in the event that none of the memory regions has an address range that includes the received address;
   a cache comprising a plurality of sets;

a replacement management table (RMT) having a plurality of entries, wherein each of the entries corresponds to one of the class identifiers and to one of the sets of the cache, and wherein the entries of the RMT are configured to store data that define the sets of the cache that may be used to store data retrieved from each of the memory regions, and wherein the RMT is coupled to receive the class identifier produced by the range register and configured to produce a tag replacement control indicia dependent on the received class identifier, wherein the tag replacement control indicia is indicative of the sets of the cache that may be used to store data retrieved from one of the memory regions having the received class identifier; and

wherein the cache is coupled to receive data retrieved from one of the memory regions and the tag replacement control indicia, and configured to store the received data in one of the sets of the cache dependent upon the tag replacement control indicia.

In view of the amendments to claim 1, Applicant points out that the similar recitations of claim 1 of the instant application and claim 1 of the co-pending application 10/655367 pointed out in the Office Action no longer exist.

With regard to Arimilli et al., applicant asserts Arimilli et al. does not teach or disclose a computing system including multiple memory regions each having a different address range and a corresponding class identifier, and a range register coupled to receive an address and configured to produce: (i) the class identifier corresponding to the memory region having an address range that includes the received address, or (ii) a default class identifier in the event that none of the memory regions has an address range that includes the received address.

In addition, Arimilli et al. does not teach or disclose a computing system including multiple memory regions each having a different address range and a corresponding class identifier, and a replacement management table (RMT) having multiple entries, wherein each entry corresponds to one of the class identifiers and to one of multiple sets of a cache, and wherein the entries of the RMT are configured to store data that define the sets of the cache that may be used to store data retrieved from each of the memory regions.

Further, Arimilli et al. does not teach or disclose a computing system including multiple memory regions each having a different address range and a corresponding class identifier, and a

replacement management table (RMT) coupled to receive a class identifier and configured to produce a tag replacement control indicia dependent on the received class identifier, wherein the tag replacement control indicia is indicative of sets of a cache that may be used to store data retrieved from one of the memory regions having the received class identifier.

Further still, Arimilli et al. does not teach or disclose a computing system including a cache having multiple sets, wherein the cache is coupled to receive data retrieved from one of multiple memory regions and a tag replacement control indicia, and wherein the tag replacement control indicia is indicative of sets of a cache that may be used to store the retrieved data, and wherein the cache is configured to store the received data in one of the sets of the cache dependent upon the tag replacement control indicia.

Applicant believes the amendments to claim 1, and the above comments regarding Arimilli et al., obviate the obviousness-type double patenting rejection of claim 1 of the instant application in view of claim 1 of the co-pending application 10/655367.

Claims 1-6 and 8-21 were rejected under 35 U.S.C. 102(e) as being anticipated by Arimilli et al. Applicant respectfully traverses this rejection. Applicant notes that claims 1, 8, 18, and 21 are independent claims. Pending claims 2-7 and 22-23 depend from claim 1, pending claims 9-10, 12-14, and 16 depend from claim 8, and pending claim 19 depends from claim 18.

Claim 1, as amended herein, is reproduced above.

With regard to claim 1 of the instant Application, applicant asserts Arimilli et al. does not teach or disclose a computing system including multiple memory regions each having a different address range and a corresponding class identifier, and a range register coupled to receive an address and configured to produce: (i) the class identifier corresponding to the memory region

having an address range that includes the received address, or (ii) a default class identifier in the event that none of the memory regions has an address range that includes the received address.

Arimilli et al. discloses a set associative cache including a cache controller, a directory, and an array including at least one congruence class containing a plurality of sets. The multiple sets of the cache are partitioned into multiple groups according to which of a plurality of information types each set can store. The sets are partitioned so that at least two of the groups include the same set and at least one of the sets can store fewer than all of the information types. The cache controller then implements different cache policies for at least two of the plurality of groups, thus permitting the operation of the cache to be individually optimized for different information types. (Arimilli et al., Abstract.)

Arimilli et al. does not teach or disclose a computing system including multiple memory regions each having a different address range and a corresponding class identifier, and a range register coupled to receive an address and configured to produce: (i) the class identifier corresponding to the memory region having an address range that includes the received address, or (ii) a default class identifier in the event that none of the memory regions has an address range that includes the received address.

In addition, with regard to claim 1 of the instant Application, Arimilli et al. does not teach or disclose a computing system including multiple memory regions each having a different address range and a corresponding class identifier, and a replacement management table (RMT) having multiple entries, wherein each entry corresponds to one of the class identifiers and to one of multiple sets of a cache, and wherein the entries of the RMT are configured to store data that define the sets of the cache that may be used to store data retrieved from each of the memory regions.

Further, with regard to claim 1 of the instant Application, Arimilli et al. does not teach or disclose a computing system including multiple memory regions each having a different address range and a corresponding class identifier, and a replacement management table (RMT) coupled to receive a class identifier and configured to produce a tag replacement control indicia dependent on the received class identifier, wherein the tag replacement control indicia is indicative of sets of a cache that may be used to store data retrieved from one of the memory regions having the received class identifier.

Further still, with regard to claim 1 of the instant Application, Arimilli et al. does not teach or disclose a computing system including a cache having multiple sets, wherein the cache is coupled to receive data retrieved from one of multiple memory regions and a tag replacement control indicia, and wherein the tag replacement control indicia is indicative of sets of a cache that may be used to store the retrieved data, and wherein the cache is configured to store the received data in one of the sets of the cache dependent upon the tag replacement control indicia.

As amended herein, claim 8 recites:

8. A method of configuring replacement eligibility of at least one set in a cache comprising a plurality of sets, the method comprising:
creating a class identifier for each of a plurality of memory regions having a different address range by class identifier creation software;
receiving an address;
using the address produce: (i) the class identifier corresponding to the memory region having an address range that includes the received address, or (ii) a default class identifier in the event that none of the memory regions has an address range that includes the received address;
using the produced class identifier to create a tag replacement control indicia through employment of a replacement management table, wherein the tag replacement control indicia is indicative of the sets of the cache that may be used to store data retrieved from one of the memory regions having the produced class identifier; and
configuring the replacement eligibility of the at least one set in the cache as a function of the tag replacement control indicia.

As amended herein, claim 18 recites:

18. A computer program product for configuring replacement eligibility of at least one set in a cache comprising a plurality of sets, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer code for creating a class identifier for each of a plurality of memory regions, wherein each of the memory regions has a different address range;

computer code for using a received address to produce: (i) the class identifier corresponding to the memory region having an address range that includes the received address, or (ii) a default class identifier in the event that none of the memory regions has an address range that includes the received address;

computer code for using the produced class identifier to create a tag replacement control indicia through employment of a replacement management table, wherein the tag replacement control indicia is indicative of the sets of the cache that may be used to store data retrieved from one of the memory regions having the produced class identifier; and

computer code for configuring the replacement eligibility of the at least one set in the cache as a function of the tag replacement control indicia.

As amended herein, claim 21 recites:

21. (Currently Amended) A processor, comprising:

a plurality of memory regions each having a different address range;

a cache comprising a plurality of sets;

computer code for creating a class identifier for each of the memory regions;

computer code for using a received address to produce: (i) the class identifier corresponding to the memory region having an address range that includes the received address, or (ii) a default class identifier in the event that none of the memory regions has an address range that includes the received address;

computer code for using the produced class identifier to create a tag replacement control indicia through employment of a replacement management table, wherein the tag replacement control indicia is indicative of the sets of the cache that may be used to store data retrieved from one of the memory regions having the produced class identifier; and

computer code for configuring the replacement eligibility of the at least one set in the cache as a function of the tag replacement control indicia.

With regard to claims 8, 18, and 21, applicant asserts Arimilli et al. does not teach or disclose configuring replacement eligibility of at least one set in a cache including multiple sets, wherein the configuring includes "creating a class identifier for each of a plurality of memory regions having a different address range by class identifier creation software;" and "using a received address to produce: (i) the class identifier corresponding to the memory region having an address

range that includes the received address, or (ii) a default class identifier in the event that none of the memory regions has an address range that includes the received address."

Further, with regard to claims 8, 18, and 21, Arimilli et al. does not teach or disclose configuring replacement eligibility of at least one set in a cache including multiple sets, wherein the configuring includes "creating a class identifier for each of a plurality of memory regions having a different address range by class identifier creation software;" "using [a] produced class identifier to create a tag replacement control indicia through employment of a replacement management table, wherein the tag replacement control indicia is indicative of the sets of the cache that may be used to store data retrieved from one of the memory regions having the produced class identifier;" and "configuring the replacement eligibility of the at least one set in the cache as a function of the tag replacement control indicia."

For at least the above reasons, Applicant asserts Arimilli et al. fails to teach or disclose all of the elements and limitations of pending independent claims 1, 8, 18, and 21. Applicant also believes that pending claims 2-7 and 22-23 the depend from claim 1, pending claims 9-10, 12-14, and 16 that depend from claim 8, and pending claim 19 that depends from claim 18, are also allowable for at least the above reasons.

Claim 7 was rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. as applied to claim 4, and further in view of Chauvel et al. (US Patent No. 6,826,652). Applicant respectfully traverses this rejection. Applicant notes that pending claims 2-7 and 22-23 depend from claim 1.

Claim 1, as amended herein, is reproduced above.

With regard to claim 1 of the instant Application, Applicant asserts the combination of Arimilli et al. and Chauvel et al. does not teach or disclose a computing system including multiple

memory regions each having a different address range and a corresponding class identifier, and a range register coupled to receive an address and configured to produce: (i) the class identifier corresponding to the memory region having an address range that includes the received address, or (ii) a default class identifier in the event that none of the memory regions has an address range that includes the received address.

Claim 1, as amended herein, is reproduced above.

Arimilli et al. is described above.

Chauvel et al. discloses a cache architecture (16) for use in a processing includes a RAM set cache for caching a contiguous block of main memory (20). The RAM set cache can be used in conjunction with other cache types, such as a set associative cache or a direct mapped cache. A register (32) defines a starting address for the contiguous block of main memory (20). The data array (38) associated with the RAM set may be filled on a line-by-line basis, as lines are requested by the processing core, or on a set-fill basis which fills the data array (38) when the starting address is loaded into the register (32). As addresses are received from the processing core, hit/miss logic (46) the starting address register (32), a global valid bit (34), line valid bits (37) and control bits (24, 26) are used to determine whether the data is present in the RAM set or whether the data must be loaded from main memory (20). The hit/miss logic (46) also determines whether a line should be loaded into the RAM set data array (38) or in the associated cache. (Chauvel et al., Abstract.)

Neither Arimilli et al. nor Chauvel et al. teaches or discloses a computing system including multiple memory regions each having a different address range and a corresponding class identifier, and a range register coupled to receive an address and configured to produce: (i) the class identifier corresponding to the memory region having an address range that includes the received address, or

(ii) a default class identifier in the event that none of the memory regions has an address range that includes the received address.

In addition, with regard to claim 1 of the instant Application, the combination of Arimilli et al. and Chauvel et al. does not teach or disclose a computing system including multiple memory regions each having a different address range and a corresponding class identifier, and a replacement management table (RMT) having multiple entries, wherein each entry corresponds to one of the class identifiers and to one of multiple sets of a cache, and wherein the entries of the RMT are configured to store data that define the sets of the cache that may be used to store data retrieved from each of the memory regions.

Further, with regard to claim 1 of the instant Application, the combination of Arimilli et al. and Chauvel et al. does not teach or disclose a computing system including multiple memory regions each having a different address range and a corresponding class identifier, and a replacement management table (RMT) coupled to receive a class identifier and configured to produce a tag replacement control indicia dependent on the received class identifier, wherein the tag replacement control indicia is indicative of sets of a cache that may be used to store data retrieved from one of the memory regions having the received class identifier.

Further still, with regard to claim 1 of the instant Application, the combination of Arimilli et al. and Chauvel et al. does not teach or disclose a computing system including a cache having multiple sets, wherein the cache is coupled to receive data retrieved from one of multiple memory regions and a tag replacement control indicia, and wherein the tag replacement control indicia is indicative of sets of a cache that may be used to store the retrieved data, and wherein the cache is configured to store the received data in one of the sets of the cache dependent upon the tag replacement control indicia.

For at least the above reasons, Applicant asserts the combination of Arimilli et al. and Chauvel et al. fails to teach or disclose all of the elements and limitations of pending independent claim 1. Applicant also believes that pending claims 2-7 and 22-23 that depend from claim 1 are also allowable for at least the above reasons.

In the present response, Applicant addresses all of the claim objections and rejections cited in the Office Action. In view of the amendments to the claims and Applicant's remarks, Applicant believes pending claims 1-10, 12-14, 16, 18-19, and 21-23 are in condition for allowance, and respectfully requests allowance of pending claims 1-10, 12-14, 16, 18-19, and 21-23.

With the amendments to the claims presented herein, there are currently 4 pending independent claims and 19 total pending claims in the application. As the original application had 4 independent claims and 21 total claims, Applicant believes no additional fees are due. In the event that any other fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of CARR LLP.

Should the Examiner deem that any further amendment is desirable to place this application in condition for allowance, the Examiner is invited to telephone the undersigned at the number listed below.

Respectfully submitted,

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